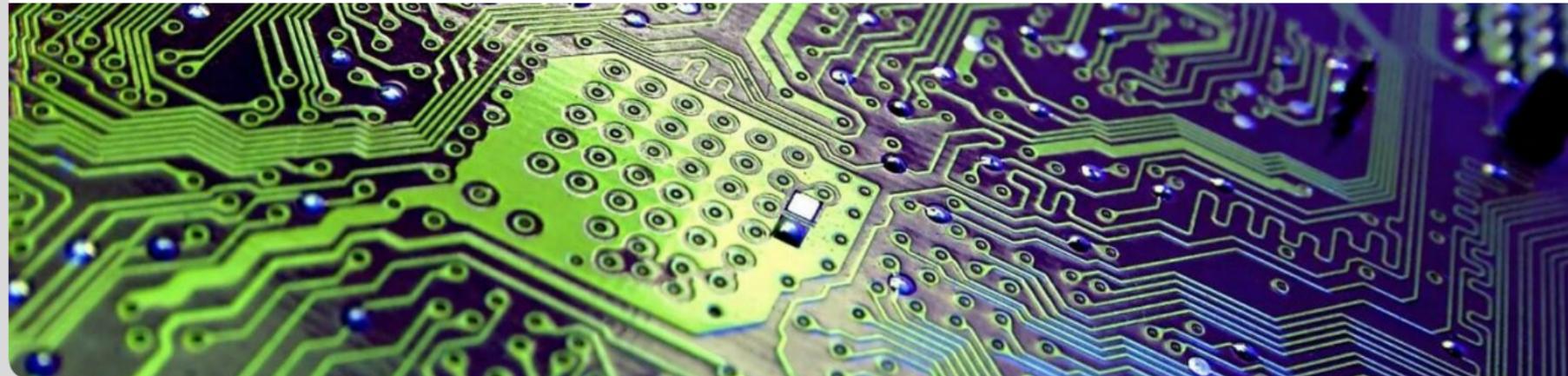


Secure sharing of FPGAs in the Cloud: New Challenges at the Technology Level

Fall School on Nano-Electronics for Secure Systems 2021

Jonas Krautter, Dennis R. E. Gnad, Mehdi B. Tahoori | 10.11.2021

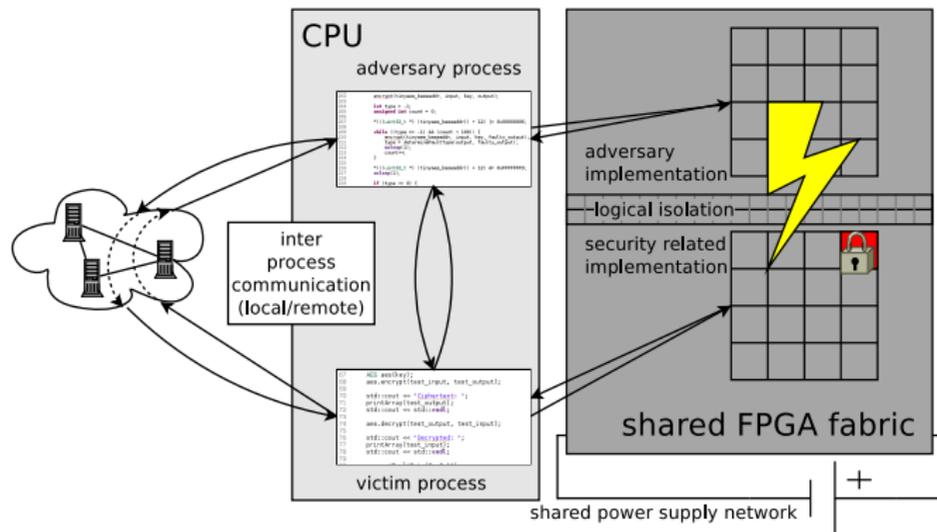
ITEC – CHAIR OF DEPENDABLE NANO COMPUTING (CDNC)



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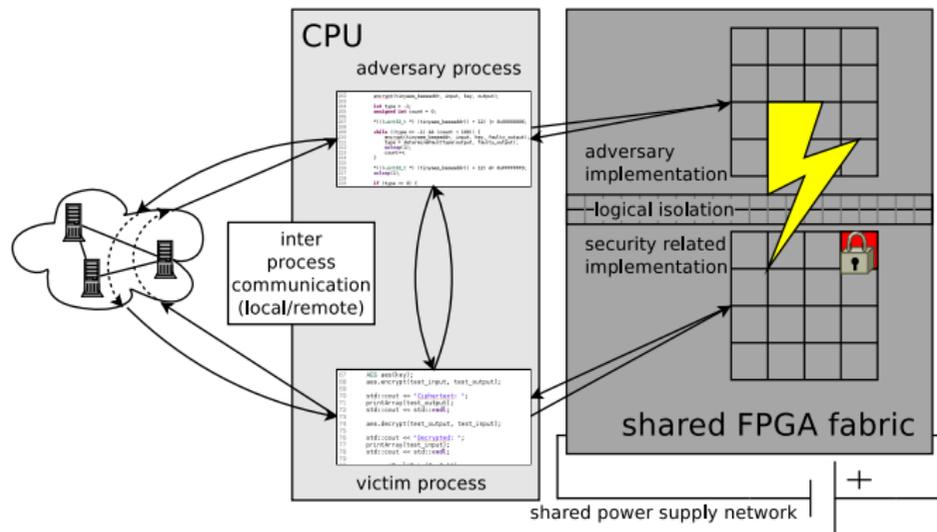
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Threat Model



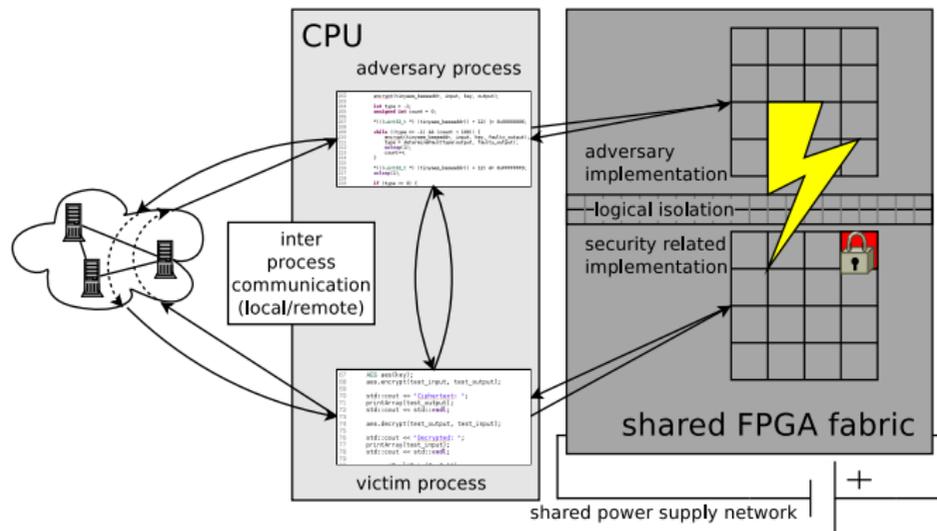
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Threat Model



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- Shared FPGA fabric ⇒ **Shared Power Supply Network**

Threat Model



- Attacker and victim design **logically isolated**
- Shared FPGA fabric ⇒ **Shared Power Supply Network**
- ⇒ **Fault attacks** from one design to the other

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Related work

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Related work

- FPGAs can be crashed with a large amount of Ring Oscillators (ROs)¹

¹Gnad et al., "Voltage drop-based fault attacks on FPGAs using valid bitstreams", FPL 2017

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Related work

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- Seemingly benign logic can be used to precisely inject faults into AES⁶

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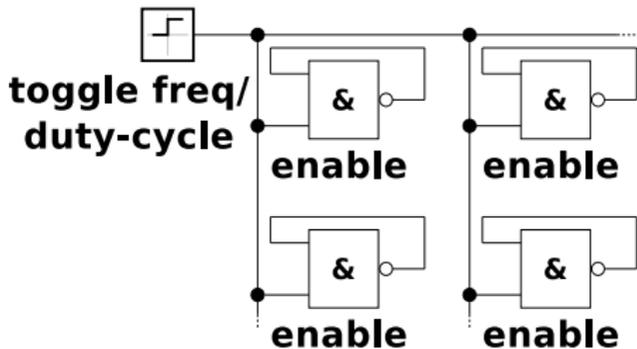
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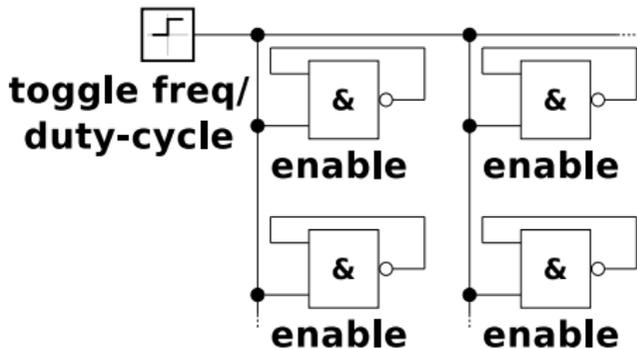
Voltage Virus Logic



- Ring Oscillators (ROs) cause high power consumption¹

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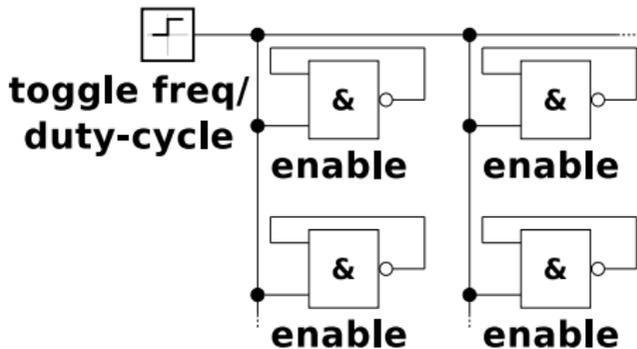
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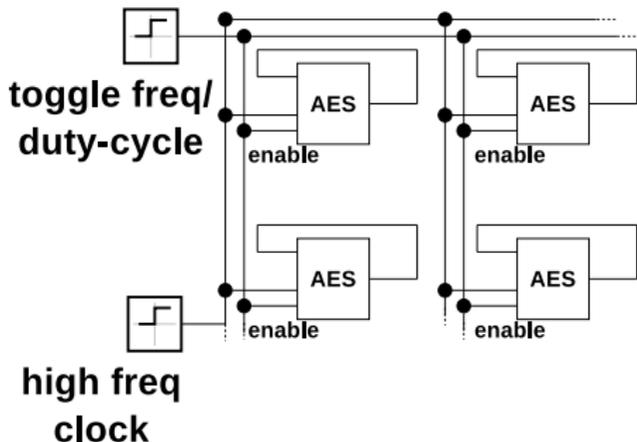
Voltage Virus Logic



- Ring Oscillators (ROs) cause high power consumption¹
- Gate switching \Rightarrow Current variation \Rightarrow Voltage fluctuations
- RO grid additionally toggled in a very specific way

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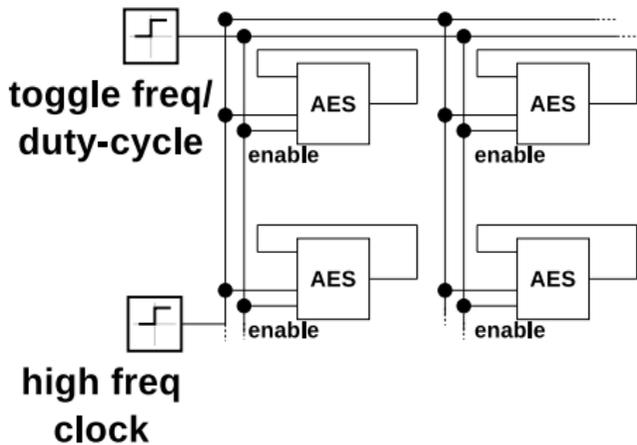
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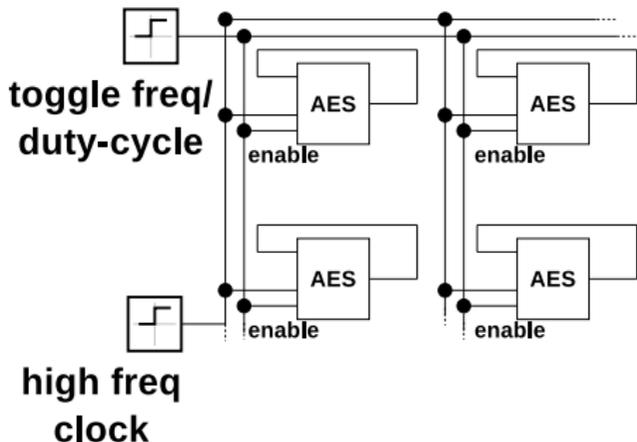
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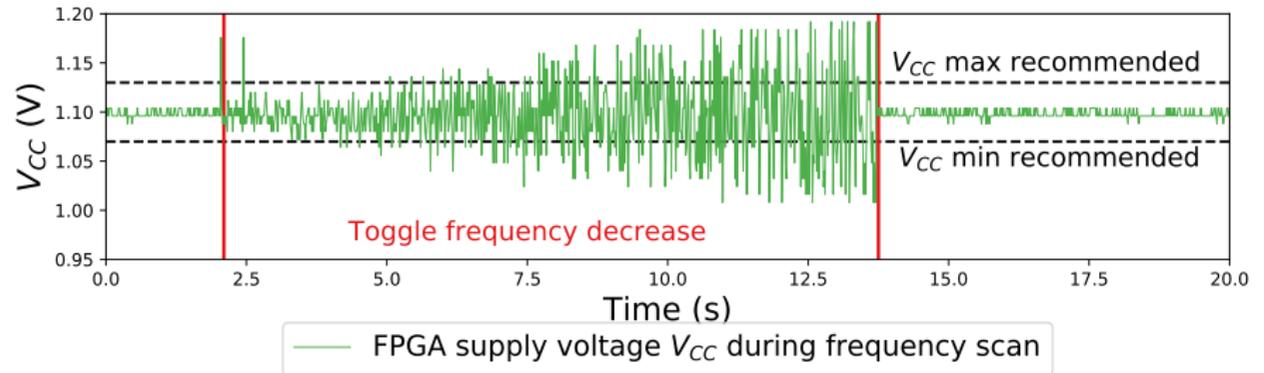
Voltage Virus Logic



- ROs can be detected \Rightarrow Use instances of non-malicious logic¹
- Sequential logic driven by a high speed clock
- Again: Common enable signal for synchronized toggling

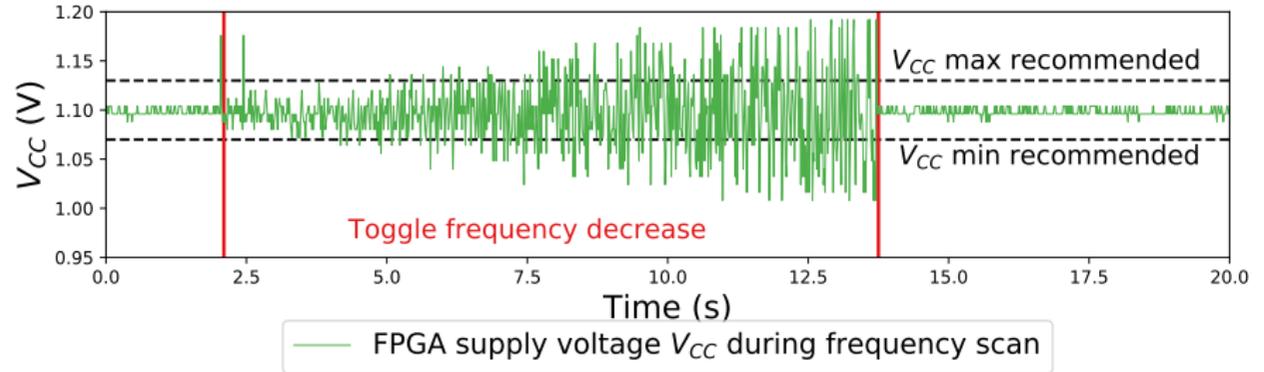
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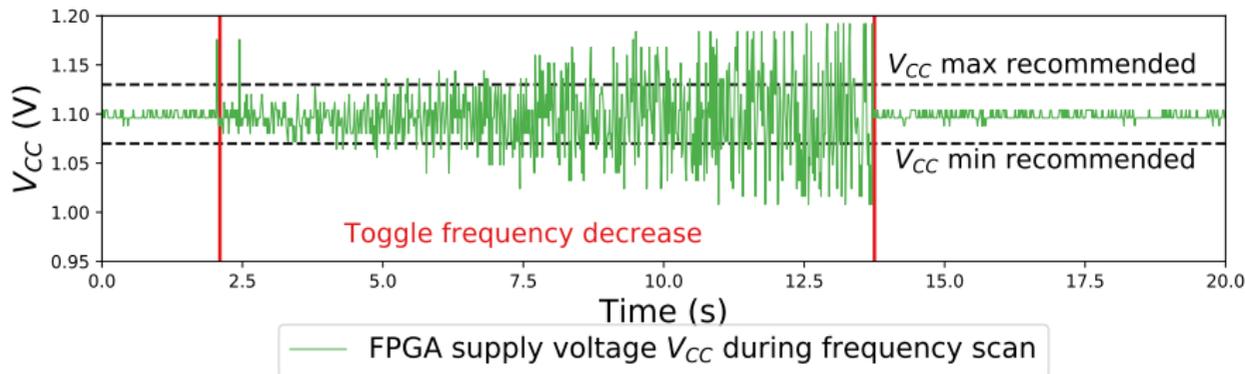
- Toggle signal controls the timing and intensity of the voltage drop

Voltage Virus Logic



- Toggle signal controls the timing and intensity of the voltage drop
- Both frequency and duty-cycle have an impact

Voltage Virus Logic



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- Both frequency and duty-cycle have an impact
- \Rightarrow **Calibration** of fault injection parameters required

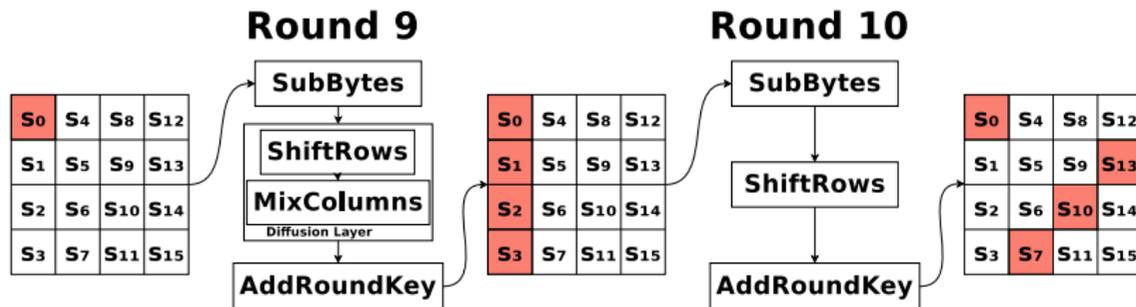
Fault Attack on AES

- Differential Fault Analysis on AES³
- Differential \Rightarrow **Pairs** (c, c') of correct and incorrect ciphertexts

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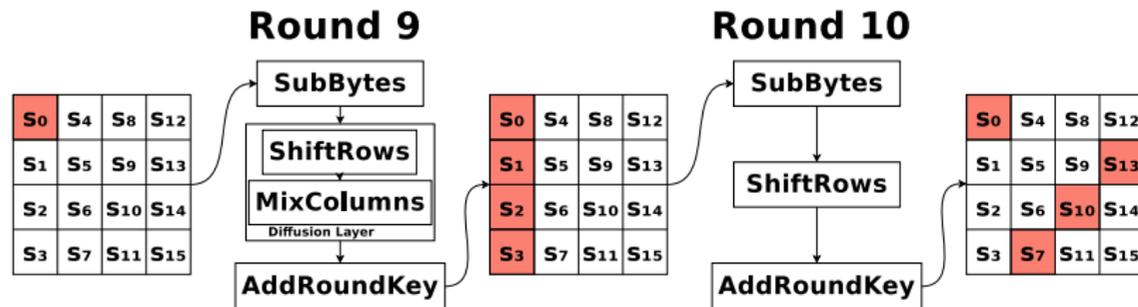
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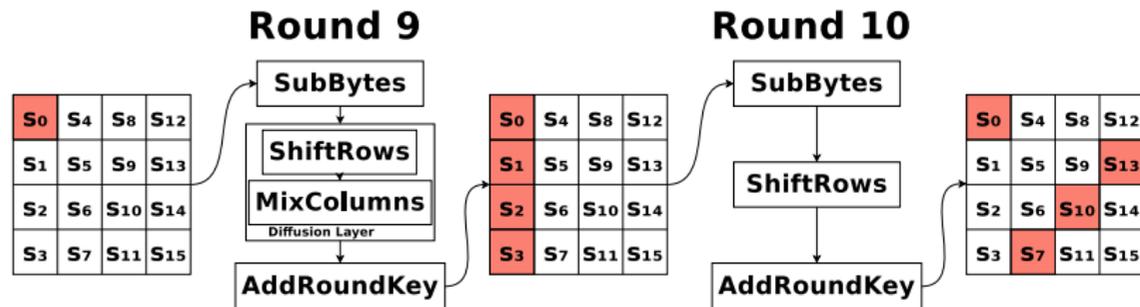


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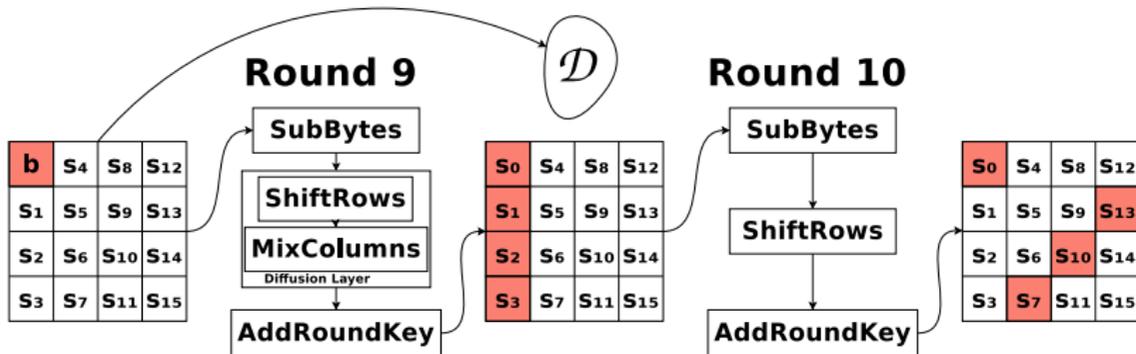
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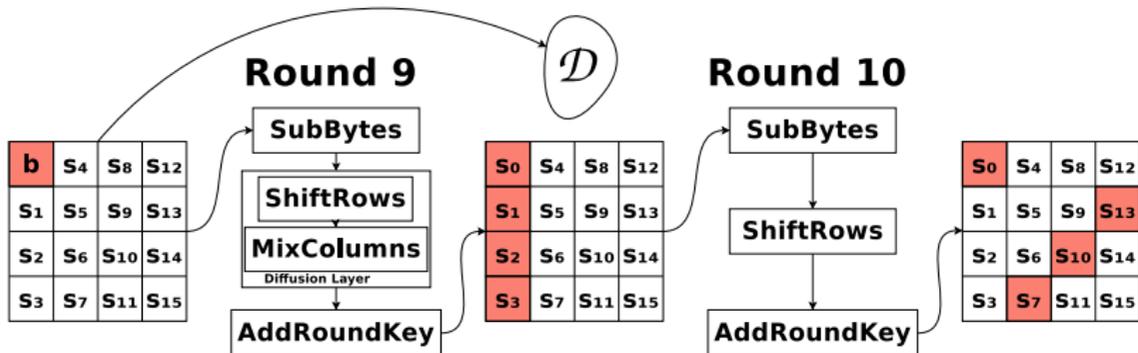
- \Rightarrow Fault model allows us to **verify** successful injection
- How do we get the secret key?

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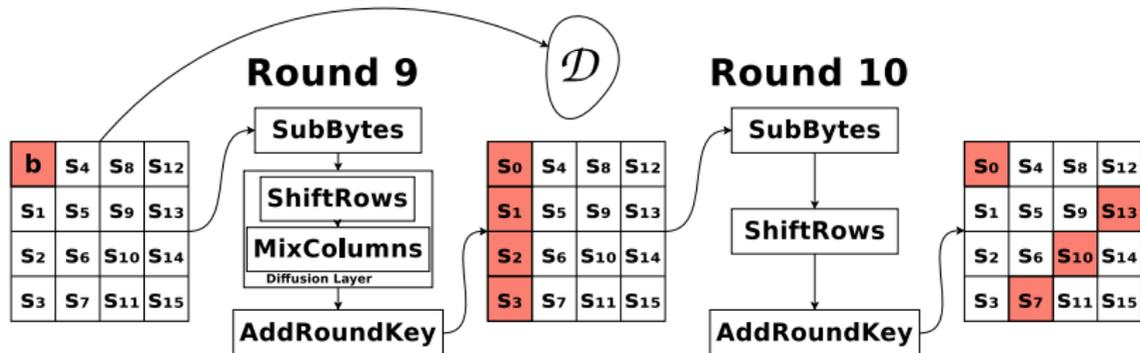
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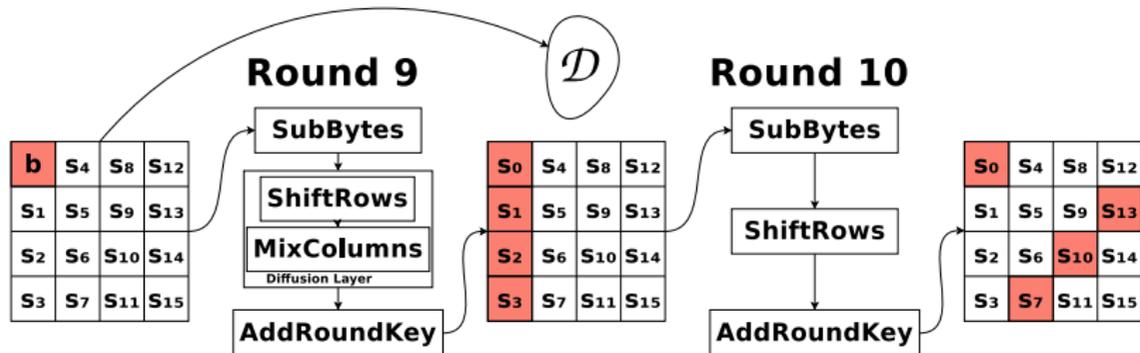
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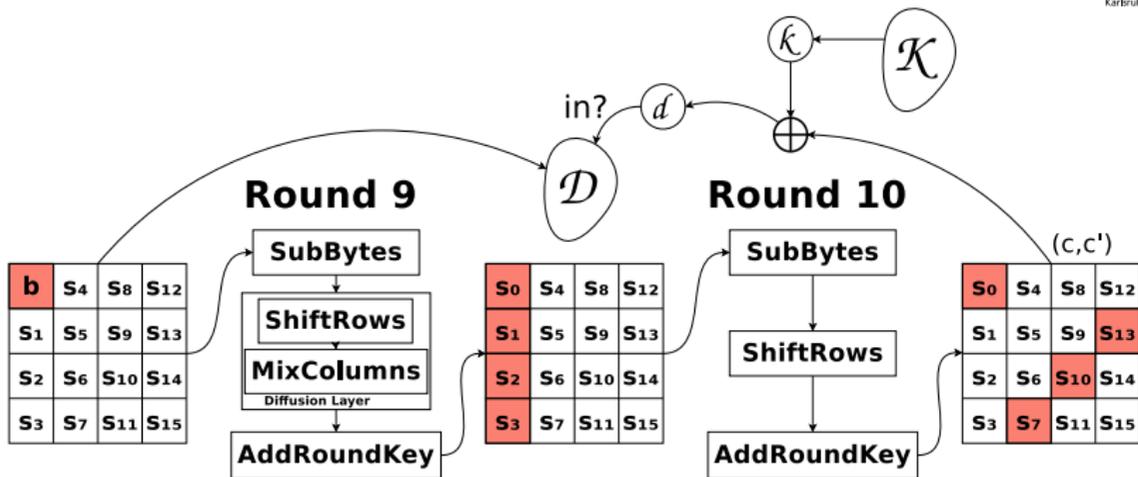
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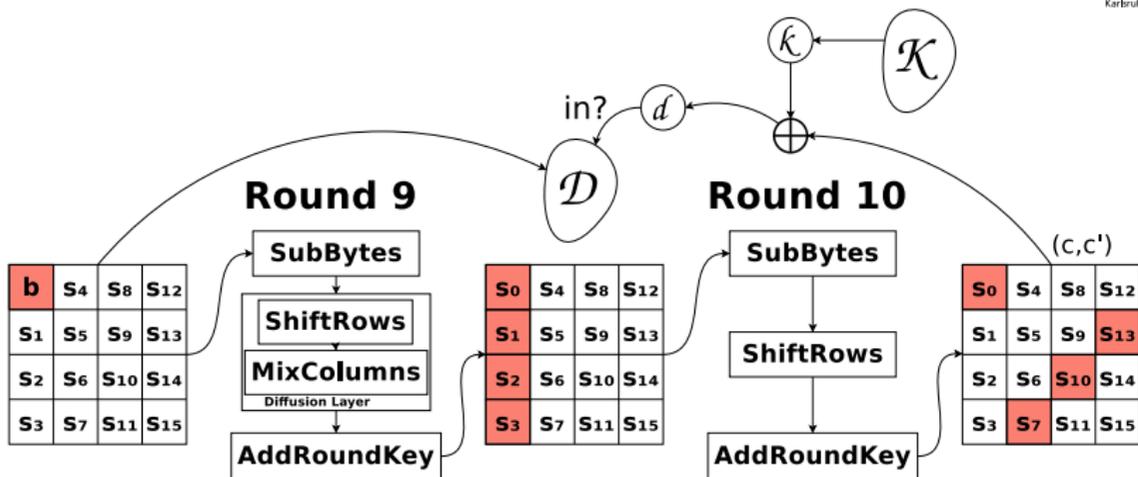
- Consider a single faulty byte $b' \neq b$ before the 9th round
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- Compute these differences into a set \mathcal{D}

Fault Attack on AES



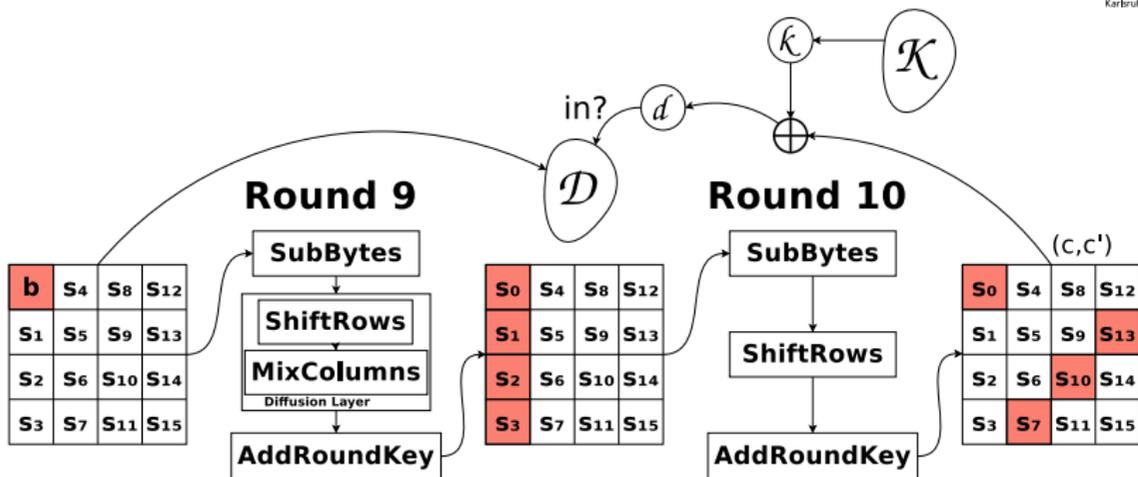
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 \Rightarrow Set of key candidates \mathcal{K}

Fault Attack on AES



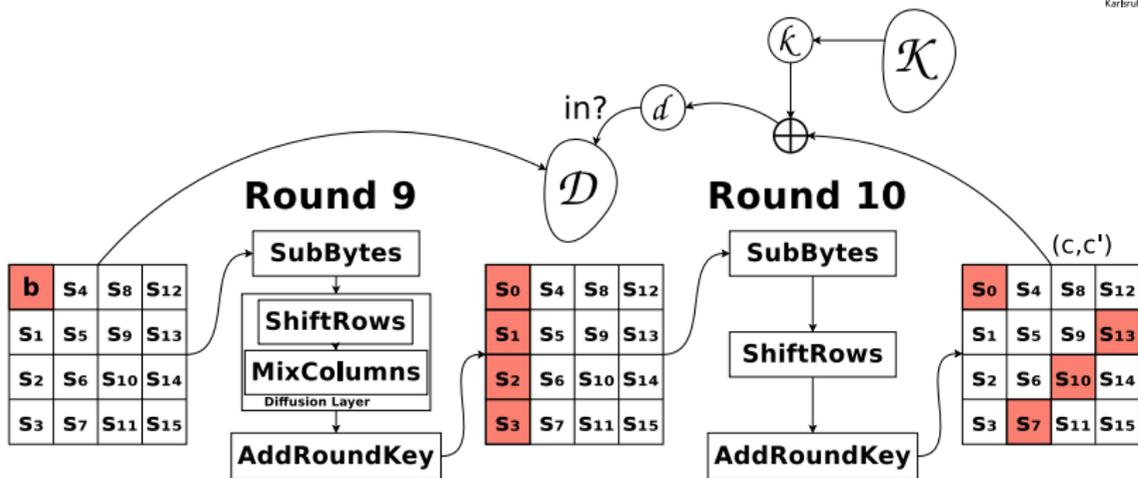
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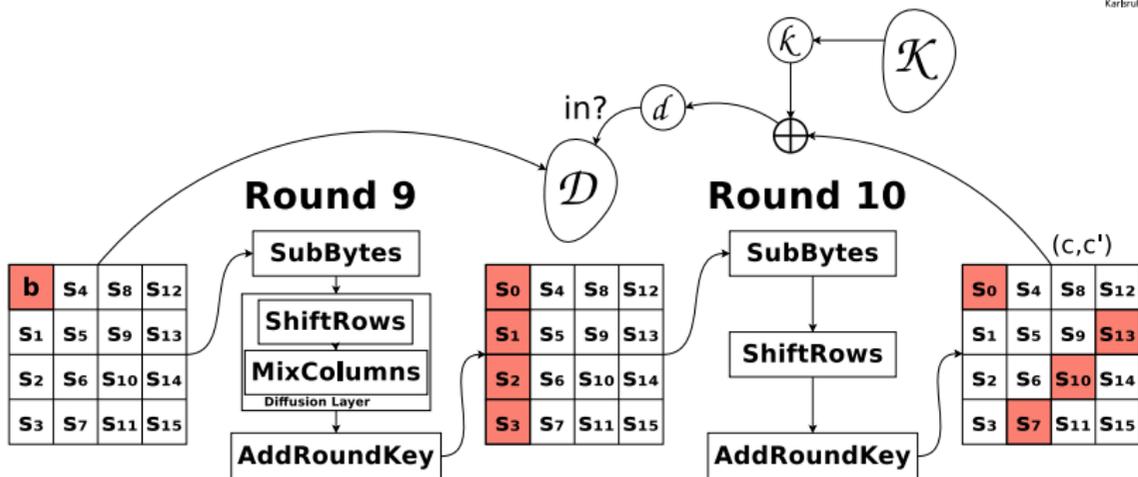
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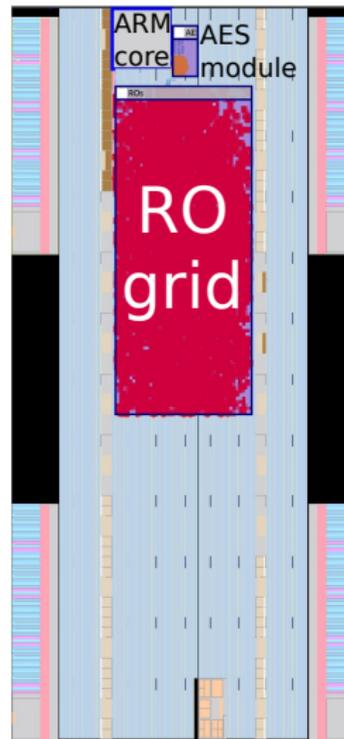
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- Repeat with a fresh pair until one key candidate remains

Secure sharing of FPGAs in
the Cloud: New Challenges
at the Technology Level

Edge and Cloud Devices

Terasic DE10-Pro – Intel Stratix 10 (2.8M LUTs):

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Edge and Cloud Devices

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Lattice iCE40-HX8K Breakout Board (8K LUTs):

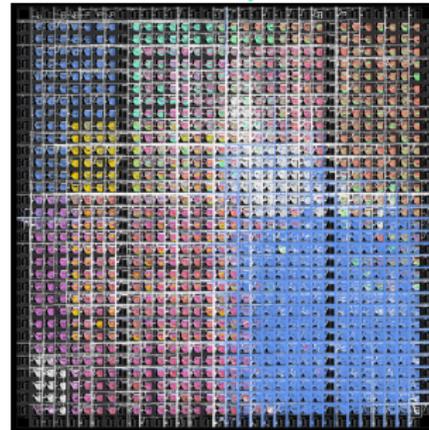


RO Group #0

RO Group #3

RO Group #7

RO Group #5



RO Group #1

RO Group #2

AES

RO Group #6

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FPGA-based fault attacks on AES

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- \Rightarrow Live-Demo on Intel Stratix 10

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Thank you for your attention!

Questions? Write us an email!

{jonas.krautter,dennis.gnad,mehdi.tahoori}@kit.edu